HALF ADDER DESIGN AND SIMULATION USING GRAPHENE NANORIBBONS AND FINFETS

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ABSTRACT

In combinational logic circuits, half adder plays an important role in computation of arithmetic units. As far as digital electronics is concerned, high processing adders have significant contribution in total delay and power of the system. This paper presents the comparison between the rise time and fall time obtained at the sum and carry outputs of the half adder deigned by the using simple interconnects, designed by using graphene nanoribbon (GNR) interconnects and also the half adders simulated using FinFET drivers and GNR interconnects.

KEYWORDS-

Half adders, Graphene Nanoribbon interconnects, FinFETs, MLGNR, SLGNR, Rise time and Fall time.

1. INTRODUCTION

According to Moore's law the number of transistors in an Integrated circuit (IC) is expected to double every year. This means that to accommodate a large number of transistors on a single IC, the dimensions of the transistors should be reduced. Also in order to perform at par with these transistors at such nano-scale regime, the interconnects used for designing of the circuit should also be downscaled. Thus a need to design the interconnects at the nano-scale technology has evolved with the recent advancements in the field of VLSI [1].

In most of the VLSI circuits, copper (Cu) interconnects are used as the interconnect technology. When these Cu interconnects are used at the nano-scale regime, they get affected by sidewall scattering and grain boundaries [2]. In order to overcome the problems raised due to copper interconnects, other feasible solutions for global interconnects where researched. One such solution emerged as Graphene nanoribbon interconnects (GNRs). The GNRs are fabricated by etching and patterning of Graphene which has the most promising properties including large mean free paths, high current densities and thermal conductivity [3].

2. TECHNOLOGIES USED

2.1 Interconnect technology: Graphene Nanoribbons

Graphene is a zero-gap material represented by carbon atoms arranged in a honey-comb structure [4]. The unzipping of carbon nanotubes and pattering of graphene both results in construction of graphene nanoribbons (GNRs). These ribbon like strips of graphene have dimensions less than 10nm [5]. Depending on their geometry the GNRs are classified as metallic or semiconducting. Also depending on their band structures, GNRs can be divided into zig-zag GNRs and armchair GNRs as shown in Figure 1. The zig-zag GNRs are always metallic in nature while armchair GNRs can be either metallic or semiconducting [6].

Futher GNRs can be classified based on the number of layers present, they can be SLGNRs (Single layer graphene nanoribbons) and MLGNRs (Multi-layer graphene nanoribbons) [7].
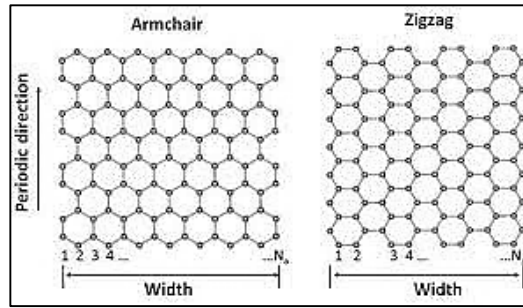

Figure 1. Armchair and zigzag GNRs

2.2 Driver technology: FinFET

FinFET is a multi-gate metal oxide semiconductor field effect transistor (MOSFET). The design of a FinFET includes a conducting channel that rises above the insulator level and creates a structure of a thin silicon, that is shaped like a fin (Figure 2). Due to this fin, number of gates can operate with a single transistor.
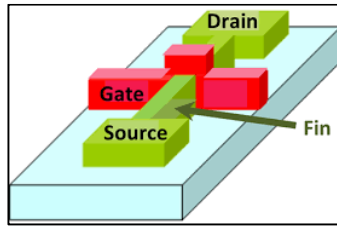

Figure 2. FinFET structure

The main advantages of using FinFET technology include reduction in short channel effects, sharper contrast between on/off states and also reduction in leakage. Usage of FinFETs provide faster switching speeds and also low power consumption [8].

Intel also designed FinFET in 2012 for its commercial use. The shape of Intel's FinFET is in the form of a triangle unlike rectangle as in usual FinFETs. The logic behind is, that a triangle has a higher structural strength as compared to a rectangle [9].
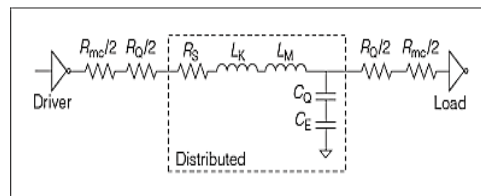
3. RLC MODEL FOR GNR INTERCONNECTS

Figure 3. RLC model representation for GNRs

The Figure 3 represents the RLC model for GNR interconnects [10].

R_Q (Quantum contact resistance) :

$$((\hbar / 2e^2) / N_{ch} . N_{layer}) = 12.94 \text{ K}\Omega / N_{ch}.N_{layer} \tag{1}$$

C_Q (Quantum capacitance) :

$$N_{ch} . N_{layer} .4e^2 / \hbar V_f) \text{ aF/}\mu\text{m} \tag{2}$$

C_E (electrostatic capacitance) :

$$\varepsilon_0 *(w/d) \text{ aF/}\mu\text{m} \tag{3}$$

I_K (Kinetic Inductance) :

$$(\hbar / 4e^2 V_f) / N_{ch} . N_{layer} \quad \text{nH/ }\mu\text{m} \tag{4}$$

I_M (magnetic Inductance) :

$$\mu_0 * (d/w) \text{ nH/ }\mu\text{m} \tag{5}$$

Where

$\hbar$ = Planck's constant (6.626×10^{-34} J.s)
e = Electronic charge (1.6×10^{-19} C)
N_{ch} = Number of conducting channels in one layer
N_{layer} = Number of GNR layers
V_f = Fermi velocity = $8*10^5$ m/s for GNR
w = width of MLGNR
d = distance from the ground.
ε_0 = $8.85* 10^{-12}$ (Electrostatic Permittivity)
μ_0 = $4\Pi *10^{-7}$ (Magnetic Permeability)
$N_{ch} = N_{ch,electron} + N_{ch,hole}$ N_{ch}
$$= \sum [1+\exp((E_{n,electron}-E_F)/k_B T)]^{-1} + \sum [1 + \exp ((E_F - E_{n, hole}) / k_B T)]^{-1} \tag{6}$$

Where $E_{n, electron}$ ($E_{n, hole}$) = minimum (maximum) energy of the nth conduction (valence) sub-band.

4. SIMULATION SETUP

In this paper Half adder circuit is first designed using normal interconnects and the rise time and fall time obtained at the outputs of the sum and carry are observed. Secondly, the same half adder circuit is redesigned using MLGNR interconnects and the difference in the outputs of the first case and second case is compared. In the last circuit of half adder the FinFET drivers are used with MLGNR interconnects. The results obtained from all the three circuit are compared and analysed.

The parasitic values for the MLGNR interconnect are calculated on the basis of the RLC model (Fig.1.3) designed and discussed in the previous section (section 3). For the purpose of calculation of RLC parameters, equations (1), (2), (3), (4) and (5) are used with the following assumptions:

N_{layer} (Number of MLGNR layers) = 10
Total number of conducting channels in one layer = 1
d (distance from the ground) = 50 nm
w (width of MLGNR) = 10 nm
l (length of MLGNR) = 10 µm
Number of Fins(M) in FinFET drivers = 2

All the simulations in this paper are performed at 16 nm scale on TSPICE software using Predictive Technology models of BSIM-CMG by BSIM group at University of California, Berkeley.
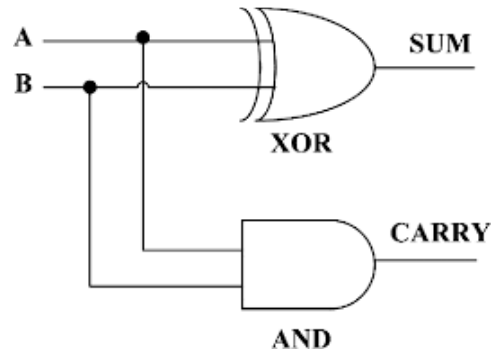
5. HALF ADDER

Figure 4. Logic circuit diagram for half adder

The half adder circuit is designed (Figure 4) using XOR and AND logic gates which provide the Sum and the carry outputs respectively [11].

Table 1.1 Truth table for half adder

A	B	Sum	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1
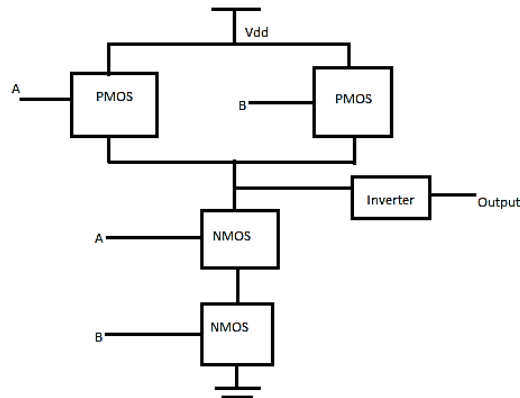
Figure 5. AND gate schematic for half adder circuit , that provides carry as the output
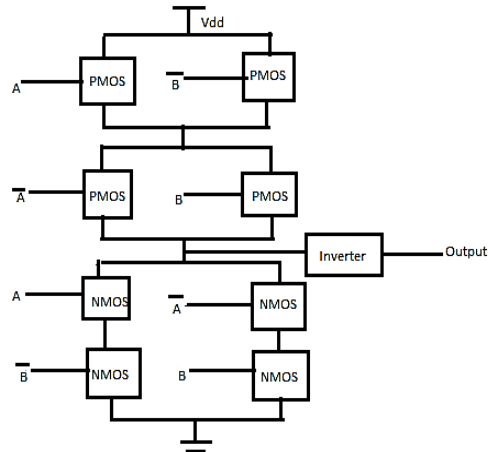
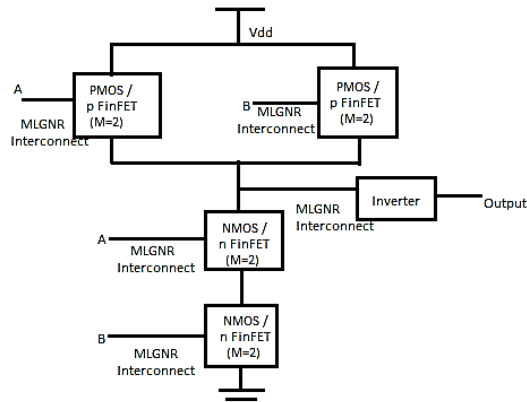Figure 6. XOR gate schematic for half adder, the output of this gate is provided as the sum of the inputs

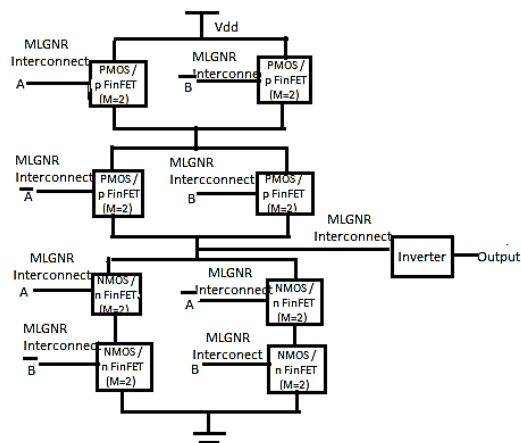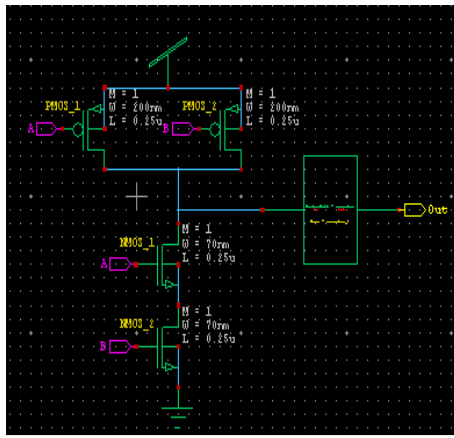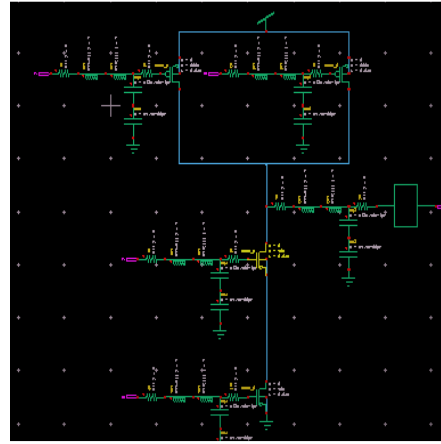Figure 7. AND gate schematic designed using 5 MLGNR interconnects / FinFET drivers

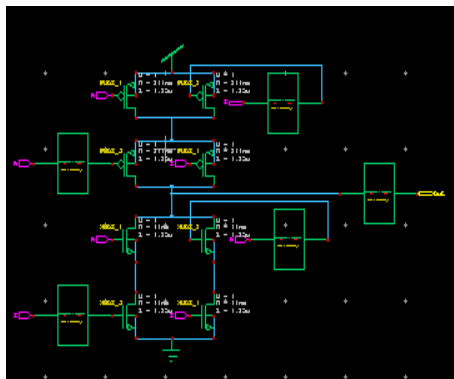Figure 8. XOR gate schematic designed using 9 MLGNR interconnects / FinFET drivers

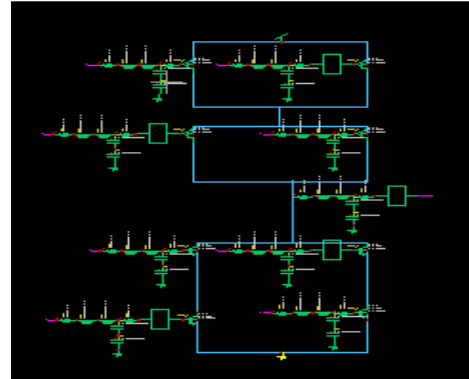Carry TSPICE schematic for simple half adder

Carry TSPICE schematic for half adder designed using MLGNRs / FinFETs

Figure 9

Sum TSPICE schematic for simple half adder

Sum TSPICE schematic for half adder designed using MLGNRs / FinFETs
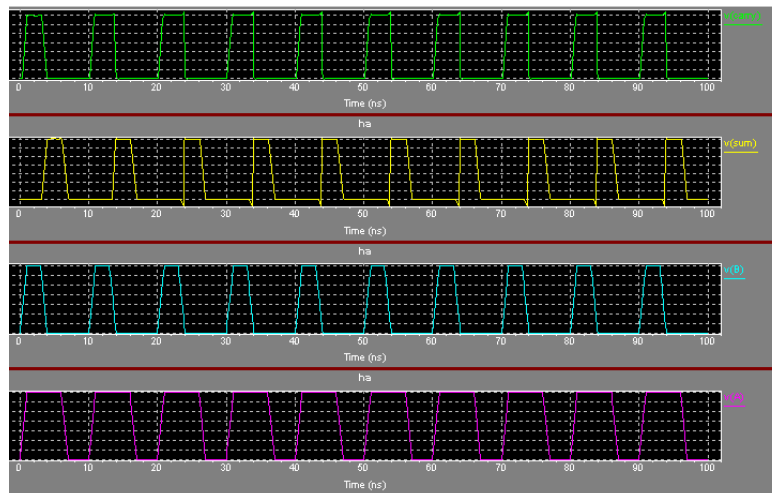
Figure 10

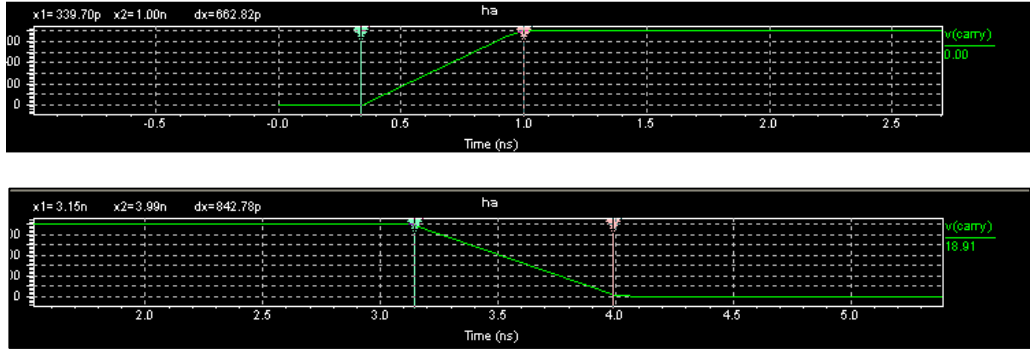Figure 11. Sum and carry output waveform for half adder

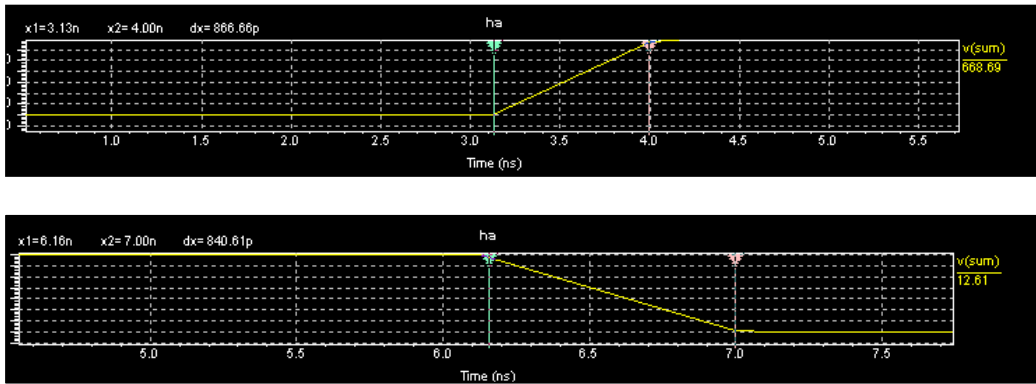Figure 12. Carry rise time and fall time for simple half adder

Figure 13. Sum rise time and fall time in case of simple half adder
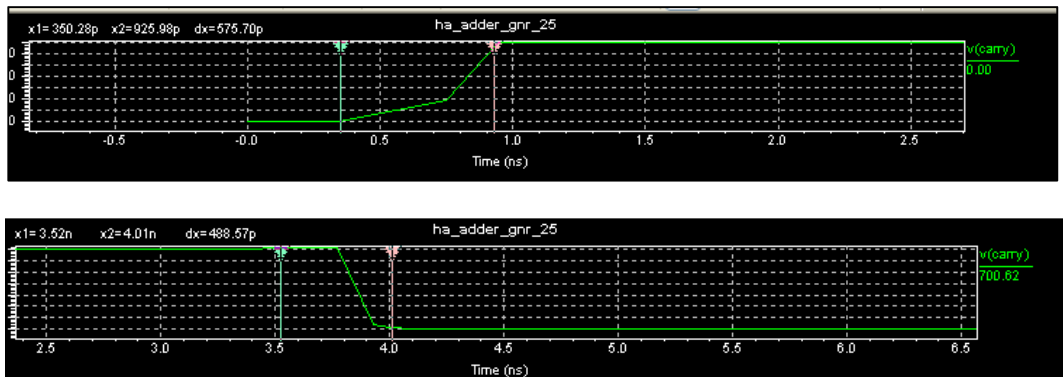

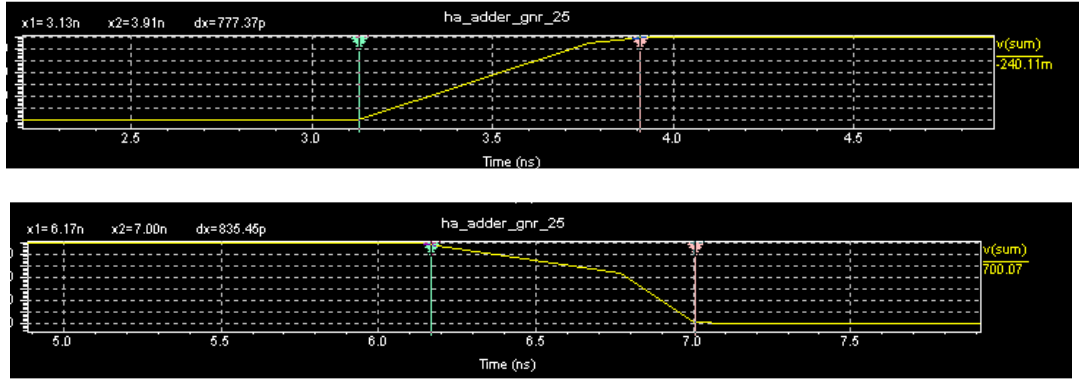Figure 14. Carry rise time and fall time for half adder designed using MLGNR interconnects

Figure 15. Sum rise time and fall time for half adder using MLGNR interconnects
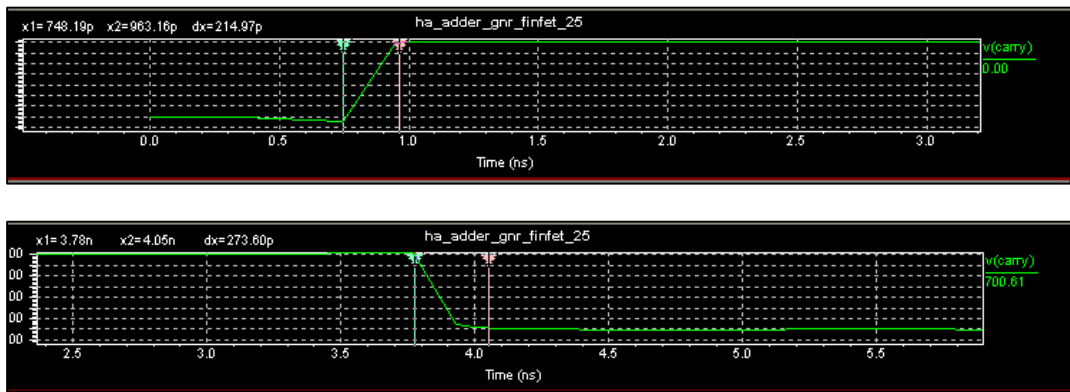

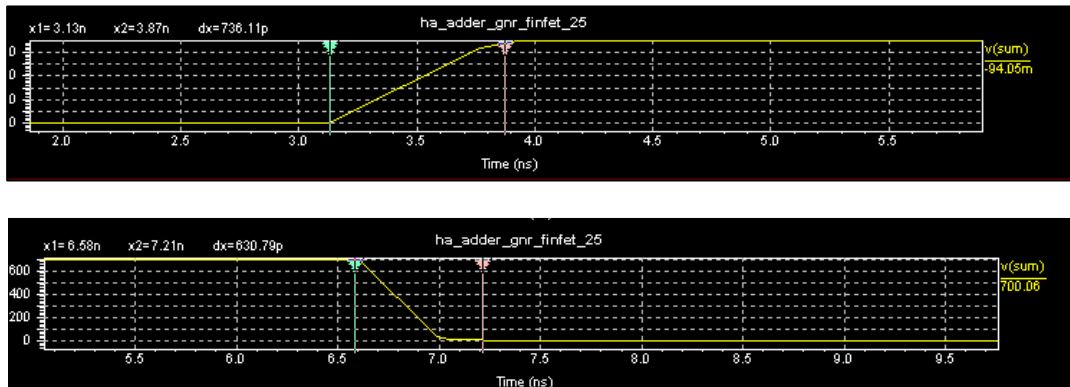Figure 16. Carry rise time and fall time for half adder designed using FinFETs and MLGNR interconnects

Figure 17. Sum rise time and fall time for half adder designed using FInFETs and MLGNR interconnects

Table 1.2 Sum and carry rise time and fall time for a half adder

	Half Adder	Half adder designed using MLGNR interconnects	Half adder designed using FinFETs and MLGNR interconnects
Rise time (Sum)	866.66 ps	777.37 ps	736.11 ps
Fall time (Sum)	840.61 ps	835.45 ps	630.79 ps
Rise time (Carry)	662.82 ps	575.70 ps	214.97 ps
Fall time (Carry)	842.78 ps	488.57 ps	273.60 ps

The above Table 1.2 shows the values of rise time and fall time obtained in all the three differently designed half adder circuits. The variation in the timings clearly show that with the incorporation of MLGNR interconnects in the half adder circuit, both the rise time and fall time are decreased. Furthermore by using FinFET drivers with GNR interconnects, a much reduction in rise and fall times is observed.

Table 1.3 Percentage improvement comparison for both rise and fall time at sum and carry

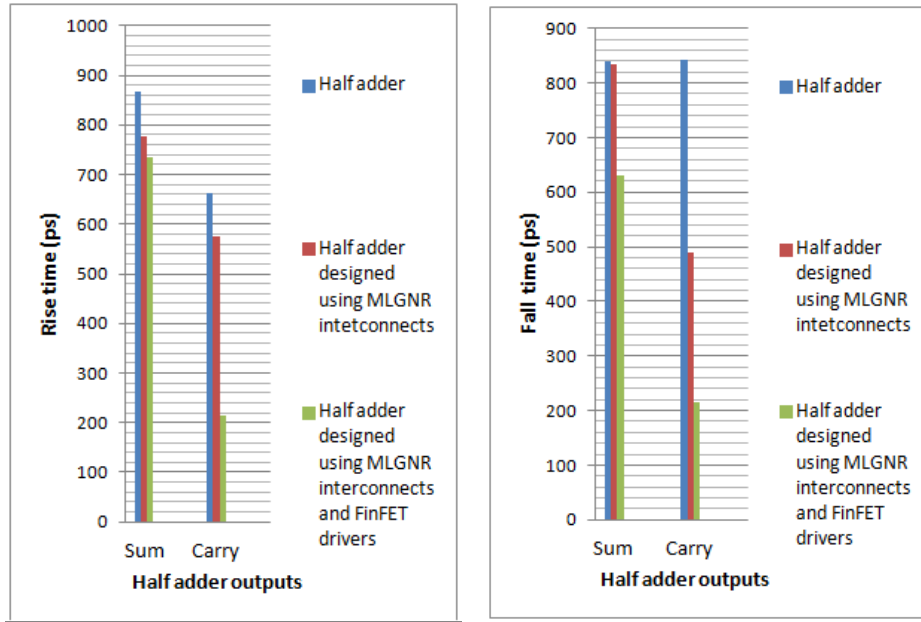| % improvement in the rise time and fall time			
	Between Half adder & Half adder designed using MLGNR interconnects	Between Half adder & Half adder designed using FinFETs and MLGNR interconnects	Between Half adder with MLGNR interconnects and Half adder designed using FinFETs and MLGNR interconnects
Rise time (Sum)	10.30	10.02	5.30
Fall time (Sum)	0.61	24.96	24.49
Rise time (Carry)	13.14	67.56	62.65
Fall time (Carry)	42.02	67.53	43.99

The percentage improvement in the rise and fall time can be understood from the above table 1.2. It is clear that if Graphene Nanoribbons and FinFETs are incorporated with the half adder circuit, an appreciable amount of reduction in the timings can be obtained.

6. RESULTS AND DISCUSSIONS

In this paper a study on half adder circuit is performed. The sum and carry outputs of the half adder are analysed on the basis of their rise time and fall time. The study is enhanced by modifying the same circuit with MLGNR interconnects and further by including FinFET drivers as well. The number of multi layer graphene nanoribbon interconnects (MLGNRs) and the

number of fins in finFET drivers can be increased or decreased according to the requirement of the designer. The embodiment of these technologies in the half adder circuit produced refined results as compared to the results obtained using a simple half adder circuit.

On an average the percentage improvement in the sum output of the circuit is 12.61% similarly in the carry output the average percentage improvement obtained is 49.48%.

Graph 1. The rise time and fall time distribution between the three half adder circuits designed in the paper.

7. CONCLUSION

The simulations performed on TSPICE, have evidently shown that Graphene nanoribbons are suitable candidate for the interconnects in digital circuits like half adder. Also, by replacing the traditional CMOS drivers with FinFET drivers has contributed in achieving a gradual decrease in the timings. A much profound study on both of these new technologies may result in obtaining prudent results in the field of VLSI.

ACKNOWLEDGEMENTS

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